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EXAMINER	
ROJAS, DANIEL E	
ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/563,040	BERTHOLD ET AL.	
	Examiner	Art Unit	
	DANIEL ROJAS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24 and 26-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24 and 26-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 23-39 and 42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 30 recites the limitation "the first….controllable [switch]" in line 6. There is insufficient antecedent basis for this limitation in the claim. For the purposes of examination, examiner will take “the first, second, and third controllable switches” to be “the second, third, and fourth controllable switches.”

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 24, 26-34 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klass (US Patent No. 5,917,355) in view of applicant admitted prior art (applicant's Figure 4), hereinafter referred to as Klass and AAPA, respectively.

7. For claim 27, Klass's invention as shown in his Figure 4 comprises a signal delay circuit (INV1) configured to generate a delayed clock signal (output of INV1) corresponding to the clock signal (CK) delayed by a time delay (INV1 has a constant inherent delay) but fails to teach the said circuit node, a programmable capacitor unit, a first isolating circuit and a second isolating circuit. However, examiner takes official notice that it is notoriously old and well known that a capacitor connected to ground at an output to any circuit serves as a filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a capacitor directly connected between ground and node X of Klass's invention in order to filter noise. Thus, the combination circuit of Klass's invention with the capacitor as described above comprises a circuit node (X) arranged to charge a capacitor (C) in a charging phase in response to the clock signal being logically low (as explained below) and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed clock signal being logically high; and a programmable capacitor unit coupling the circuit node (X, Figure 4 above) to a reference potential (ground). For Figure 4 above, when the clock signal is logically low, transistor P1 is on, allowing capacitor C to charge. The capacitor C discharges only when the clock signal (CK), input D, and the delayed clock signal (CKD) are both high. AAPA teaches a latch circuit (slave latch and the transmission gate TG). Therefore, it would have been

obvious to substitute Klass's slave latch (303) with AAPA's slave latch (slave latch and TG) since it has been held that the substitution of one known element for another would have yielded predictable results one of ordinary skill in the art at the time invention (as explained below). Both Klass' slave latch (303) and AAPA's slave latch receive an output signal from a dynamic master latch and hold the logical value at the output based on the clock signal. Therefore, the combination of the modified version of Klass (with a capacitor, as defined above) with AAPA's circuit comprises a first isolating circuit (TG) configured to be clocked by the clock signal and having an input connected to the circuit node (as described above); a second isolating circuit (clocked inverter within the slave latch) configured and arranged to be clocked by the delayed clock signal (as described below); wherein an output of the first isolating circuit feeds back to the input of the first isolating circuit via the second isolating circuit (as shown). The delayed clock signal (output of INV1) is equal to the clock signal received by the second isolation circuit (inverted input terminal receiving the clock signal).

8. For claim 24, the combination of Klass and AAPA as defined above further teaches that the circuit node is arranged to discharge in the evaluation phase in response to the data signal being logically high and the circuit node is arranged to not discharge in the evaluation phase in response to the data signal being logically low (inherent based upon the structure).

9. For claim 26, the combination of Klass and AAPA as defined above further teaches a slave latch circuit (slave latch); wherein the first isolating circuit has an output connected to the slave latch circuit (as shown), the first isolating circuit is configured to

generate an output signal at the output, and the slave latch circuit is configured to buffer-store the output signal (inherent based upon the structure).

10. For claim 28, the combination circuit of Klass and AAPA as defined above inherently teaches the signal delay circuit, the circuit node, and the programmable capacitor unit being incorporated into a master latch.

11. For claim 29, the combination of Klass and AAPA as defined above further teaches that the master latch circuit further includes an inverter (P1, as explained below) configured to generate an and inverted clock signal corresponding to an inversion of the clock signal (as explained below); the master latch circuit further includes a first controllable switch (401) driven by the inverted clock signal; and the first controllable switch switches the operating voltage to the circuit node in response to the clock signal being logically low (inherent based upon the structure). When the clock signal is high, the output of P1 will be low. When the clock signal is low, the output of P1 will be high. Therefore, P1 acts as an inverter. Nand gate 401 is a switch controlled by two inputs wherein it is inherently controlled by the output of P1. Therefore, nand gate 401 is driven by the inverted clock signal (produced by P1).

12. For claim 30, the combination of Klass and AAPA as defined above further teaches that the master latch circuit further includes a reference potential node (source terminal of N3) configured to be coupled to a reference potential (ground); the master latch circuit further includes a second, third and fourth controllable switches, the second (N1), third (N2) and fourth (N3) controllable switches being connected in series with one another between a voltage supply (VDD) and the reference potential node (as shown).

13. For claim 31, the combination of Klass and AAPA as defined above further teaches that the master latch circuit is configured to generate a delayed inverted clock signal (via P1, as explained below) and to drive the second controllable switch with the delayed inverted clock signal (as explained below). When the clock signal is high, the output of P1 will be low. When the clock signal is low, the output of P1 will be high. Therefore, P1 acts as an inverter. It is noted that there is a constant inherent delay caused by the switching of P1. Nand gate 401 is a switch controlled by two inputs wherein it is inherently controlled by the output of P1. Since the output of 401 controls the second controllable switch, the output of P1 inherently drives the second controllable switch.

14. For claim 32, the combination of Klass and AAPA as defined above further teaches that the third controllable switch is arranged to be driven by the data signal (D, as shown).

15. For claim 33, the combination of Klass and AAPA as defined above further teaches that the fourth controllable switch is arranged to be driven by the clock signal (CK, as shown).

16. For claim 34, the combination of Klass and AAPA as defined above further teaches that the capacitor is connected in parallel with the second, third and fourth controllable switches (inherent, as explained above).

17. For claim 37, the combination of Klass and AAPA as defined above further teaches that a circuit that is capable of use wherein the master latch circuit is configured

to make the time delay less than a time period of the clock signal (the functionality does not define the structure over the prior art).

18. For claim 38, the combination of Klass and AAPA as defined above teaches the limitations of claim 28 but fails to teach that the signal delay circuit comprises a plurality of inverter delay stages. It is known that adding a plurality of delay stages would increase the delay value. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a plurality of inverter delay stages to increase the delay time. Furthermore, it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

19. For claim 39, the combination of Klass and AAPA as defined above inherently teaches that the master latch circuit is configured to receive only a single supply voltage.

20. Claims 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klass.

21. For claim 35, Klass's invention as shown in his Figure 4 comprises a signal delay circuit (INV1) configured to generate a delayed clock signal (output of INV1) corresponding to the clock signal (CK) delayed by a time delay (INV1 has a constant inherent delay) but fails to teach the said circuit node and a programmable capacitance unit. However, examiner takes official notice that it is notoriously old and well known that a capacitor connected to ground at an output to any circuit serves as a filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention to include a capacitor directly connected between ground and node X of Klass's invention in order to filter noise. Thus, the combination circuit of Klass's invention with the capacitor as described above comprises a circuit node (X) arranged to charge a capacitor (C) in a charging phase in response to the clock signal being logically low (as explained below) and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed clock signal being logically high; and a capacitor with a programmable capacitance (see paragraph 4 of this action) coupling the circuit node (X, Figure 4 above) to a reference potential (ground). For Figure 4 above, when the clock signal is logically low, transistor P1 is on, allowing capacitor C to charge. The capacitor C discharges only when the clock signal (CK), input D, and the delayed clock signal (CKD) are both high. It is inherent from the structure of the combination that the signal delay circuit, the circuit node, and the programmable capacitor unit are incorporated into a master latch circuit. However, the modified version of Klass (i.e. adding the capacitor) fails to teach that the time delay is adjustable. However, it is known to use a variable delay line in place of a constant delay in order to increase the flexibility of the circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to replace Klass' inverter INV1 with a variable delay line since it has been held that the provision of adjustability, where needed, involves only routine skill in the art. In re Stevens, 101 USPQ 284 (CCPA 1954).

22. For claim 36, Klass's invention as shown in his Figure 4 comprises a signal delay circuit (INV1) configured to generate a delayed clock signal (output of INV1)

corresponding to the clock signal (CK) delayed by a time delay (INV1 has a constant inherent delay) but fails to teach the said circuit node and a programmable capacitance unit. However, examiner takes official notice that it is notoriously old and well known that a capacitor connected to ground at an output to any circuit serves as a filter. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include a capacitor directly connected between ground and node X of Klass's invention in order to filter noise. Thus, the combination circuit of Klass's invention with the capacitor as described above comprises a circuit node (X) arranged to charge a capacitor (C) in a charging phase in response to the clock signal being logically low (as explained below) and to discharge in an evaluation phase depending on a data signal in response to the clock signal being logically high and the delayed clock signal being logically high; and a capacitor with a programmable capacitance (see paragraph 4 of this action) coupling the circuit node (X, Figure 4 above) to a reference potential (ground). For Figure 4 above, when the clock signal is logically low, transistor P1 is on, allowing capacitor C to charge. The capacitor C discharges only when the clock signal (CK), input D, and the delayed clock signal (CKD) are both high. It is inherent from the structure of the combination that the signal delay circuit, the circuit node, and the programmable capacitor unit are incorporated into a master latch circuit; wherein during the evaluation phase the capacitor discharges with a time constant in response to the data signal being logically high and the time constant is less than the time delay (the modified version of Klass as defined above is capable of performing this function and therefore does not distinguish the structure over the prior art).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANIEL ROJAS whose telephone number is (571)270-5070. The examiner can normally be reached on Monday-Friday 7:30-8 EST, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

/D. R./
Examiner, Art Unit 2816